

**ABSTRACT**

An electrically programmable transistor fuse having a double-gate arrangement disposed in a single layer of polysilicon in which a first gate is disposed overlapping a portion of a source region and a second gate is insulated from the first gate and disposed overlapping a portion of a drain region. The first gate includes a terminal for receiving an externally applied control signal and the second gate is capacitively couple to the drain region in which a coupling device is included for increasing the capacitive coupling of the second gate and the drain region for enabling reduction in fuse programming voltage.